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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
YASUSHI INAGAKI, ET AL	: EXAMINER: GETACHEW, AIBY
SERIAL NO: 10/522,335	:
FILED: JANUARY 25, 2005	: GROUP ART UNIT: 2841
FOR: MULTILAYER PRINTED WIRING BOARD	:

APPEAL BRIEF UNDER 37 C.F.R. §41.31

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

This is an appeal from a final Office Action dated June 15, 2007. A Notice of Appeal was timely filed on December 17, 2007.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is IBIDEN CO., Ltd., 1, Kandacho 2-chome, Ogaki-shi, Gifu 503-8604, Japan.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative and the assignees are aware of no appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1-20 are pending, stand rejected and are herein appealed.

IV. STATUS OF THE AMENDMENTS

In a Final Office Action dated June 15, 2007, the Examiner finally rejected Claims 1-20. The attached Appendix VIII reflects Claims 1-20 as presently pending on appeal.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Claim 1 is directed to a multilayer printed wiring board (e.g., item 10 in Fig. 6; Applicants' specification at p. 20, lines 6-12) that includes a core substrate (e.g. item 30 in Fig. 6; Applicants' specification at p. 20, lines 12-16) and a first conductor layer (e.g. item 34P in Fig. 6; Applicants' specification at p. 20, lines 12-16) having conductor circuits (e.g. item 34 in Fig. 6; Applicants' specification at p. 20, lines 12-16) formed on the core substrate. An interlayer insulating layer (e.g. item 50 in Fig. 6; Applicants' specification at p. 20, lines 20-25) is formed over the first conductor layer and the core substrate, a second conductor layer having conductor circuits (e.g. item 58 in Fig. 6; Applicants' specification at p. 20, lines 20-25) is formed on the interlayer insulating layer. A via hole structure (e.g. item 60 in Fig. 6; Applicants' specification at p. 20, lines 20-25) electrically connects one of the conductor circuits of the first conductor layer and one of the conductor circuits of the second conductor layer (e.g. shown in Fig. 6), and the first conductor layer on the core substrate has a thickness which is larger than a thickness of the second conductor layer on the interlayer insulating layer (Applicants' specification at p. 21, lines 8-13).

Claim 6 is directed to a multilayer printed wiring board (e.g., item 10 in Fig. 19; Applicants' specification at p. 45, lines 12-16) having a core substrate including a multilayer core substrate with not less than three layers (e.g., item 30 in Fig. 19; Applicants'

specification at p. 45, lines 16-17). The not less than three layers includes one or more inner conductor layers (e.g., item 16E in Fig. 19; Applicants' specification at p. 45, lines 23-27) having conductor circuits (e.g., item 16 in Fig. 19; Applicants' specification at p. 45, lines 23-27). Also recited in Claim 6 is a conductor layer having conductor circuits (e.g., items 34P and 34 in Fig. 19; Applicants' specification at p. 45, lines 18-21) formed over the core substrate, an interlayer insulating layer (e.g., item 50 in Fig. 19; Applicants' specification at p. 47, lines 6-11) formed over the conductor layer and the core substrate, and a through hole structure (e.g., item 36 in Fig. 19; Applicants' specification at p. 47, lines 3-5) formed through the interlayer insulating layer and electrically connecting one of the conductor circuits of the inner conductor layer and one of the conductor circuits of the conductor layer formed over the core substrate (e.g., shown in Fig. 19). The inner conductor layer of the core substrate and the conductor layer over the core substrate include a power supply layer or an earth (e.g., Applicants' specification at p. 45, line 27 – p. 46, line 3).

Claim 18 recites a multilayer printed wiring board (e.g., item 10 in Fig. 6; Applicants' specification at p. 20, lines 6-12) that includes a core substrate (e.g. item 30 in Fig. 6; Applicants' specification at p. 20, lines 12-16). Also included is a multilayered structure formed on the core substrate and including a first conductor layer (e.g. item 34P in Fig. 6; Applicants' specification at p. 20, lines 12-16) having a plurality of conductor circuits (e.g. item 34 in Fig. 6; Applicants' specification at p. 20, lines 12-16) formed on the core substrate, at least one interlayer insulating layer (e.g. item 50 in Fig. 6; Applicants' specification at p. 20, lines 20-25) formed over the first conductor layer, and a second conductor layer having a plurality of conductor circuits (e.g. item 158 in Fig. 6; Applicants' specification at p. 20, lines 20-25) formed on the at least one interlayer insulating layer and the core substrate. Also included is a second conductor layer having conductor circuits (e.g. item 58 in Fig. 6; Applicants' specification at p. 20, lines 20-25) formed on the interlayer insulating layer, and a

via hole structure (e.g. item 160 in Fig. 6; Applicants' specification at p. 20, lines 25-27) electrically connecting one of the conductor circuits of the first conductor layer and one of the conductor circuits of the second conductor layer (e.g. shown in Fig. 6).

GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

A. Rejection of Claims 1-20 under 35 U.S.C. 102(b) as being anticipated by US Patent Publication No. 2004/0108862 to Azuma et al.

VII. ARGUMENTS

A. Claims 1-20 are not anticipated under 35 USC §102(b) by Azuma et al.

i. Azuma et al. does not teach all of the limitations of independent Claim 1

Azuma et al. discloses a multilayer printed wiring board and a method for detecting defects in an inner layer of the multilayer wiring board. Fig. 19A of Azuma et al. shows a multilayer printed wiring board 170 having a waste substrate portion 71B and a product portion 71A. As seen in Fig. 23A of Azuma et al., the product portion 71A is constructed of interlayer insulating layers $70A_{1-4}$ and $70B_{1-3}$, and grounding lines 76_{1-4} formed between respective pairs of the interlayer insulating layers $70A_{1-4}$ and $70B_{1-3}$. Transmission lines 74_{1-4} are connected to vias 175_{2-4}.

The Final office action takes the position that Figure 23 A of Azuma et al. discloses that "a thickness of the conductor layer (Figure 23 A Element 70 A2) on said core substrate (Figure 23 A Element 70 B2) is larger than a thickness of the conductor layer (Figure 23 A Element 70 A1) on the interlayer insulating layer (Figure 23 A Element 70 B1)."[1] As noted above, however, Figure 23A of Azuma et al. shows layers $70A_1$, $70A_2$, interlayer insulating

[1] The Final Office Action, pages 2-3. Figure 29A is reproduced as "Fig. 23A" in the Final office action and shows a similar structure to Fig. 23A with the insulating layers 70A and 70B being adjacent to one another.

layers, not as conductor layers. The layers made of conductive materials in Fig. 23A are represented by the transmission line 74_3 and the grounding line (ground layer) 76_3. However, nowhere does Azuma et al. describe that the transmission line 74_3 be made thicker than the grounding line (ground layer) 76_3.

Therefore, Azuma et al. does not teach "a first conductor layer ...; a second conductor layer ..., wherein said first conductor layer on said core substrate has a thickness which is larger than a thickness of said second conductor layer on said interlayer insulating layer," as recited in independent Claim 1.

ii. Azuma et al. does not teach all of the limitations of independent Claim 6

As noted above, Fig. 23A of Azuma et al. shows a ground or transmission layer interposed between insulating layers. However, there is no indication of a multilayer core substrate having an inner conductor layer having a plurality of conductor circuits. Indeed, Fig. 23A does not disclose the recited conductor circuits at all. Therefore, Azuma et al. does not disclose "a core substrate comprising a multilayer core substrate comprising not less than three layers including at least one inner conductor layer having a plurality of conductor circuits ..., wherein the at least one inner conductor layer of said core substrate ... include[s] a power supply layer or an earth," as recited in independent Claim 6.

Nor does Azuma et al. show the transmission line 74_3 being electrically connected to the grounding line (ground layer) 76_3 through a viahole connection. Accordingly, Azuma et al. also fails to teach "a through hole structure formed through said interlayer insulating layer and electrically connecting one of said conductor circuits of said at least one inner conductor layer and one of said conductor circuits of said conductor layer formed over said core substrate," as recited in independent Claim 6.

ii. Azuma et al. does not teach all of the limitations of independent Claim 18

Claim 18 recites "a multilayered structure formed on said core substrate and including a first conductor layer having a plurality of conductor circuits formed on said core substrate, at least one interlayer insulating layer formed over said first conductor layer, and a second conductor layer having a plurality of conductor circuits formed on said at least one interlayer insulating layer, wherein said first conductor layer on said core substrate has a thickness which is larger than a thickness of said second conductor layer on said at least one interlayer insulating layer."

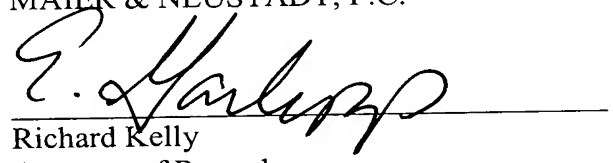
As noted above, Fig. 23A of Azuma et al. discloses interlayer insulating layers $70A_{1-4}$ and $70B_{1-3}$, and grounding lines 76_{1-4} formed between respective pairs of the interlayer insulating layers $70A_{1-4}$ and $70B_{1-3}$. Transmission lines 74_{1-4} are connected to vias 175_{2-4}. Thus, Claim 18 is also distinguishable from Azuma et al. Therefore, Azuma et al. does not teach "a multilayered structure ... including a first conductor layer ...; a second conductor layer ..., wherein said first conductor layer on said core substrate has a thickness which is larger than a thickness of said second conductor layer on said interlayer insulating layer," as recited in independent Claim 18.

B. CONCLUSION.

For the foregoing reasons, independent Claims 1, 6 and 18 are not anticipated by Azuma et al.. Furthermore, since Claims 2-5, 7-17, 19 and 20 depend directly or indirectly from one of Claims 1, 6 and 18, these dependent claims also are not anticipated by Azuma et al.. Therefore, the rejection of Claims 1-20 should be withdrawn.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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VIII. CLAIMS APPENDIX

Claim 1: A multilayer printed wiring board comprising:

a core substrate;

a first conductor layer having a plurality of conductor circuits formed on said core substrate;

an interlayer insulating layer formed over said first conductor layer and said core substrate;

a second conductor layer having a plurality of conductor circuits formed on said interlayer insulating layer; and

a via hole structure electrically connecting one of said conductor circuits of said first conductor layer and one of said conductor circuits of said second conductor layer,

wherein said first conductor layer on said core substrate has a thickness which is larger than a thickness of said second conductor layer on said interlayer insulating layer.

Claim 2: The multilayer printed wiring board according to claim 1, wherein said thickness of said first conductor layer on said core substrate is $\alpha 1$, said thickness of said second conductor layer on said interlayer insulating layer is $\alpha 2$, and $\alpha 1$ and $\alpha 2$ satisfy $\alpha 2 < \alpha 1 < 40\alpha 2$.

Claim 3: The multilayer printed wiring board according to claim 1, wherein said thickness of said first conductor layer on said core substrate is $\alpha 1$, said thickness of said second conductor layer on said interlayer insulating layer is $\alpha 2$, and said $\alpha 1$ satisfies $2\alpha 2 < \alpha 1 < 40\alpha 2$.

Claim 4: The multilayer printed wiring board according to claim 1, wherein the first conductor layer on said core substrate comprises a power supply layer or an earth.

Claim 5: The multilayer printed wiring board according to claim 1, further comprising a capacitor mounted over said second conductor layer.

Claim 6: A multilayer printed wiring board comprising:

a core substrate comprising a multilayer core substrate comprising not less than three layers including at least one inner conductor layer having a plurality of conductor circuits;

a conductor layer having a plurality of conductor circuits formed over said core substrate;

an interlayer insulating layer formed over said conductor layer and said core substrate; and

a through hole structure formed through said interlayer insulating layer and electrically connecting one of said conductor circuits of said at least one inner conductor layer and one of said conductor circuits of said conductor layer formed over said core substrate,

wherein the at least one inner conductor layer of said core substrate and the conductor layer over said core substrate include a power supply layer or an earth.

Claim 7: The multilayer printed wiring board according to claims 6, wherein said at least one inner conductor layer of said core substrate comprises the power supply layer or the earth, and said conductor layer is formed on a surface of said core substrate and comprises a signal line.

Claim 8: A multilayer printed wiring board according to claim 6, wherein the at least one inner conductor layer of said core substrate has a thickness which is larger than a thickness of the conductor layer formed over the surface of said core substrate.

Claim 9: The multilayer printed wiring board according to claim 6, wherein the at least one inner conductor layer of said core substrate comprises not less than two inner conductor layers.

Claim 10: The multilayer printed wiring board according to claim 6, wherein said core substrate comprises an electrically isolated metallic plate, and a plurality of insulating layers formed on surfaces of said electrically isolated metallic plate, respectively, said at least one inner conductor layer of said core substrate comprises a plurality of inner conductor layers, and the inner conductor layers are formed on the insulating layers, respectively.

Claim 11: The multilayer printed wiring board according to claim 6, wherein the conductor layer is formed on a surface of said core substrate, and said at least one inner layer of said core substrate has a thickness which is larger than a thickness of the conductor layer formed on the surface of said core substrate.

Claim 12: The multilayer printed wiring board according to claim 2, wherein the first conductor layer formed on said core substrate comprises a power supply layer or an earth.

Claim 13: The multilayer printed wiring board according to claim 2, further comprising a capacitor mounted over a surface of said core substrate.

Claim 14: A multilayer printed wiring board according to claim 7, wherein said at least one inner layer of said core substrate has a thickness which is larger than a thickness of the conductor layer formed on said core substrate.

Claim 15: The multilayer printed wiring board according to claim 7, wherein said at least one inner conductor layer of said core substrate comprises not less than two inner conductor layers.

Claim 16: The multilayer printed wiring board according to claim 7, wherein said core substrate comprises an electrically isolated metallic plate and a plurality of insulating layers formed on surfaces of said electrically isolated metallic plate, respectively, said at least one inner conductor layer of said core substrate comprises a plurality of inner conductor layers, and the inner conductor layers are formed on the insulating layers, respectively.

Claim 17: The multilayer printed wiring board according to claim 6, further comprising a second conductor layer having a plurality of conductor circuits formed over said interlayer insulating layer, wherein said conductor layer is formed on a surface of said core substrate, said at least one inner layer of said core substrate has a thickness which is larger than a thickness of the conductor layer formed on the surface of said core substrate, and the thickness of said conductor layer formed on the surface of said core substrate is larger than a thickness of said second conductor layer.

Claim 18: A multilayer printed wiring board comprising:

a core substrate; and

a multilayered structure formed on said core substrate and including a first conductor layer having a plurality of conductor circuits formed on said core substrate, at least one interlayer insulating layer formed over said first conductor layer, and a second conductor layer having a plurality of conductor circuits formed on said at least one interlayer insulating layer,

wherein said first conductor layer on said core substrate has a thickness which is larger than a thickness of said second conductor layer on said at least one interlayer insulating layer.

Claim 19: The multilayer printed wiring board according to claim 18, wherein said thickness of said first conductor layer on said core substrate is $\alpha 1$, said thickness of said second conductor layer on said interlayer insulating layer is $\alpha 2$, and $\alpha 1$ and $\alpha 2$ satisfy $\alpha 2 < \alpha 1 < 40\alpha 2$.

Claim 20: The multilayer printed wiring board according to claim 18, wherein said thickness of said first conductor layer on said core substrate is $\alpha 1$, said thickness of said second conductor layer on said interlayer insulating layer is $\alpha 2$, and said $\alpha 1$ satisfies $2\alpha 2 < \alpha 1 < 40\alpha 2$.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.